Electronic Packaging
An overview of mechanics and materials challenges

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Outline
• Introduction to Electronic packaging
• Key market trends and its impact on packaging
• Mechanics/materials challenges
• Emerging challenges
• summary
PC + Cell Phone Volumes

**Personal Computers**

**Phone/Smartphones**

- > 1 billion per year
- 200 million smartphones per year
- India adds 17 millions users per month!

Very high volume; portable PC/smartphones are fastest growing markets!!
Electronic package: Bridge between silicon and the world

Transistor

IC (Si Chip) or CPU

Package

Board

System
Traditional Role of Electronic Packages

- Integrated heat spreader
- Silicon die
- Package Substrate
- Mother Board
- Interconnects

Power/heat Removal
Protect the Silicon

Power Delivery
Interconnect/Geometric Scaling
Key Trends
Trends in Integrated Circuits

1/1,000,000 the size; 1/10,000,000 the weight; 1/1,000,000 the cost
10,000,000x the performance and reliability

Silicon Scaling Drives Geometric Scaling of the package; smaller length scales, tighter interconnect pitches.....
Computing + Communications Today

Data Anytime, Anywhere

@ the Office

Cellular: Voice + Data

@ Home

Broadband

@ Hotspots

Everywhere Else

10/100/GbE

802.x

@ the Office

@ Home

intell
Internet: How Do People Use Their PCs?

Enjoy Online and Offline Gaming

Share Photos With Your Community

Watch Online and Offline HD/BD Video

Create Videos to Share on YouTube*

*Other names and brands may be claimed as the property of others
Where is the Internet Going?

Even More Performance

Better Graphics

HD Quality Content

Faster Networks
Increase in Parallelism

- Instruction level parallelism
- Hyper-Threading
- Dual Core
- Quad-Core
- 10’s to 100’s of cores
Impact on Electronic Packaging
Electronic Packaging

Smaller Form Factors (handheld segment)

Larger Form Factors (performance based)

Severe constraints on “z” height total thickness: < 1mm

Electronic packaging now ALSO a product DIFFERENTIATOR compared to product ENABLER
Packaging – Doing Things Differently

Innovations in Packaging Enabling Performance & Growth

- Mainstream PC
  - Laptop/Nettop Packaging 65% smaller
- Consumer Electronics
  - Packaging 80% smaller
- Mainstream PC/All in one
  - Packaging 50% smaller
- Laptop/Nettop
  - Packaging 65% smaller
- Consumer Electronics
  - Packaging 80% smaller

Innovations enabling more product performance

Innovations enabling new market segments

Package Size

Time

Innovations in Packaging Enabling Performance & Growth
Drivers Impacting Electronic Packaging Requirements

- **The 4Fs:** Form Factor, Features, Functionality, Flexibility
  - Increase in the mobility segment w/ ubiquitous networks: thin n’ lite
  - Integration of memory, graphics, multi-bus protocols, etc

- **Environmental Concerns**
  - Energy efficiency at the component and system levels
  - The next Green initiative (Pb-Free, HF) => Materials & Assembly options

- **Increased customer expectations for Reliability**
  - Mobility use requirements; Blade servers; Etc

- **Cost / affordability**
  - Also impacts how technologies are developed and deployed
Mapping to key challenges

Typical High Performance Electronic Package

- Heat Sink
- IHS
- TIM 1 Conductive Particles
- TIM 2 Polymer Matrix
- Package
- Die (Chip)

Typical Low Power Electronic Package

- “Z” ht

Mechanical and Material
- Thermal (removal of heat/thermal density)
- Electrical (optimal power delivery/impact of multi-core)
- Cost
- Etc...

Chip Temperature Map
Key Mechanics and Materials Issues
Wide Geometric & Material Ranges

nm to mm/cm range

Die

Brittle

Die substrate core

Copper

Transistors

Cu

Elastic-plastic-creep

C4 joint

BGA (≈600μm)

Die backend

≈5μm

≈100μm

≈750μm

≈1100μm

≈2000μm

Visco-elastic

(underfills/TIM/substrates)

Package substrate

Composite (substrates & FR4)

Motherboard
Wide Range of Loading Conditions

- Different environments
  - Internal assembly
  - Shipping and handling
  - Customer assembly
  - End use (power cycling, drop, end user handling,...)

- Wide range of loads or "stresses"
  - Moisture
  - Time-temperature exposures
  - Board flexure (transient bend)
  - Shock (dynamic bend)
  - Compressive enabling loads
  - Vibration

Courtesy: S. Sahasrabudhe
Wide Range of Potential Failures
Different characteristics or driver for each

*Silicon Backend Fails*
Fracture in low-k dielectric within Si backend during assembly

*Silicon Fracture*
Die crack in T/C and interfacial delam during moisture exposures

*Interfacial Delam*

*Substrate Failures*
Via Delamination

*BGA Interconnect Failure*
Failures in Shock

Need to Understand and Quantify these Failure Modes
Mechanical Analysis Strategy

Numerical Analysis

Geometric Domain

Material Properties

Numerical Analysis
FEA Solver

Commercially available codes

Stress, strain, other metrics

Predictability

Failure Criteria

Experimental

Material Characterization

Validation

Failure Limits, Rel Data
Example 1: Si-Package Interaction

Low-K Inner Layer Dielectric in Si Back End + Pb Free solder

- Low-K (capacitance) ILD required to reduce “RC” delay in circuit.
- Pb-free solder required for environmental concerns
- Mechanically,
  - Low-K ILD is fragile
  - Pb-Free solders very stiff
Si-Package Interaction: contd.

Substrate shrinks more than die while cooling

Pkg CTE: 17 PPM/°C

Si CTE: 2.8 PPM/°C

Result: Stress management challenge
Assembly induced Stress Vs Si BE Strength

- Stress induced Si BE
- Si BE Strength

Fundamental understanding led to:
- design, material and process optimization;
- significant IP generated;
- Intel was first company to launch low-K with Pb-free solders in High volume manufacturing.
Example 2: Shock and Vibration

Acceleration at the component can exceed 1000g leading to BGA failure (Interconnect between package and motherboard)
S & V: Material/Design based solutions

- Material based
  - Intermetallic compound (IMC) quality determines joint strength
  - Engineering optimum IMC is the challenge

- Design based
  
  Red dots are experimental measurements (HSC)

System layout optimized to reduce stress on critical joint
Experimental Mechanics Lab Capabilities

**Material Char.**
- Quasi-Static properties
- Viscoelastic
- Solder properties
- Moisture Related
- Interfacial Testing

**Structural Testing**
- Bond Strength Metrologies
- Quick Turn Monitors
- Die Strength
- Rapid Temp. Cycle

**Photo-Mechanics**
- Die & Substrate Warpage
- Model Validation
- Thermo-mechanical deformation measurement
Electronic packaging transition from an enabler to also a differentiator

Proliferation and extension across traditional and new market segments and opportunities provides packaging/assembly multiple technical, business and cost challenges

Increasing demands on improved quantification and understanding of Mechanical and Materials Response along with thermal and electrical aspects.
Back Up
Materials Challenges

- New materials developed in response to Performance, Manufacturing, Environment & Cost demands
  -- Silicon level (ex.: Low--K ILD)
  -- Thermal interface materials (New polymer formulations)
  -- New solder materials (Pb--free, Low--temp alloys, etc.)
  -- Green Computing
    - Halogen Free, Flame Retardant, High Temperature Stability, etc.

- Long term time & temperature dependent data is essential
  -- Material stack ranges from linear elastic to highly viscoelastic behaviors
  -- Constitutive Properties

- Mechanics lab develops metrologies to characterize the material behaviors as needed.
Material Characterization Challenges

Example: Solder Properties

Bulk solder properties as a function of **temperature**

Solder properties as a function of **strain rate**

Joint strength as a function of rate and mode-mix

Creep properties

**Structural/Material Testing**
- Traditional Load-frame based
- Micro-tensile testing
- Nano-indentor
- Torsional Testing
- Strain Gauge Testing
- Bump/Ball Pull & Shear
Solder Joint Reliability
Impression creep rates vs particle size during aging (Pb Free)

Microstructure dependence of creep

- both particle size and grain size increase upon aging
- creep rate may increase due to particle coarsening
- creep rate not dependent on grain size

*: observed increase is due to particle coarsening
Photo-Mechanics: Interferometry based techniques validation purpose

Displacement field: Numerical analysis

Displacement field: Experimental validation

FEA model of package
Roadmap for In-Plane Displacement Measurement

Whole Pkg/BGA

Current capability

C4

Targeted AOI: Die backend

Disp. resolution (nm)

Spatial resolution (um)

Displacement resolution

Spatial resolution

Moiré Interferometry

Microscopic Moiré Interferometry (MMI)

Enhanced MMI

Nano-scale Moiré Interferometry

Optical DIC

SEM based DIC

Significant investment made on DIC (thermal) based techniques

Optical limit for spatial resolution

Current capability

50nm

208 nm

52 nm

9 nm

1 nm

0.001um

417nm

50um

In-house

In-house

SRS funding

On-going UMCP/USC

Whole Pkg/BGA

C4

Targeted AOI: Die backend

Optical DIC

SEM based DIC

Significant investment made on DIC (thermal) based techniques

Optical limit for spatial resolution